

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The specification has been amended as follows:

On page 2, between lines 6 and 7, insert the following:

1. Field of the Invention

On page 2, between lines 11 and 12, insert the following:

2. Description of the Related Art

The paragraph beginning on page 5, line 13 has been amended as follows:

BRIEF DESCRIPTION OF THE [INVENTION] DRAWINGS

The paragraph beginning on page 8, line 2, has been amended as follows:

The bonding wire 4, on the other hand, may be formed of a wire of gold or aluminum having a diameter of 25 - 30 μm and is bonded to the electrode 8a or 8b by using an ordinary wire bonding apparatus. In the present invention, a first bonding process is conducted to the electrode pad 8a on the chip, followed by a second bonding process that is conducted to the electrode pad 8b, for reducing the overall height of the semiconductor device 5.

U.S. Patent Application Serial No. 09/768,174

Paragraph beginning on page 13, line 19, has been amended as follows:

In the BGA device of the present embodiment, the bonding wires 14 are used to connect the corresponding electrode pads 18a and the electrode pads 18b at a central part of the chip 12, as indicated in FIG. 8. Further, the BGA semiconductor device of the present invention is laterally surrounded by the resin potting [1] 11.

In the Claims:

Claims 11 and 16 have been amended as follows:

11. (Amended) A semiconductor device, comprising:
a semiconductor chip having a top surface, said semiconductor chip carrying a first electrode;
a circuit substrate attached to a top surface of said semiconductor chip, said circuit substrate carrying thereon a predetermined conductor pattern including a second electrode and a third electrode;
a solder resist layer provided on said circuit substrate;
a resin layer intervening between said top surface of said semiconductor chip and said circuit substrate;
a spherical electrode [provided] formed in an opening in said solder resist layer on said

U.S. Patent Application Serial No. 09/768,174

circuit substrate in correspondence to said third electrode;

a bonding wire electrically interconnecting said second electrode of said predetermined conductor pattern on said circuit substrate and said first electrode on said semiconductor chip;
and

a resin potting encapsulating said bonding wire including said first and second electrodes, said chip and said resin potting being defined by a common edge surface substantially perpendicular to a principal surface of said substrate.

16. (Amended) A semiconductor device, comprising:

a semiconductor chip having a top surface, said semiconductor chip carrying a first electrode;

a circuit substrate [attached to] provided on a top surface of said semiconductor chip with a separation therefrom, said circuit substrate carrying thereon a predetermined conductor pattern including a second electrode and a third electrode;

a spherical electrode provided on said circuit substrate in correspondence to said third electrode;

a bonding wire electrically interconnecting said second electrode of said predetermined conductor pattern on said circuit substrate and said first electrode on said semiconductor chip;

a resin potting encapsulating said bonding wire including said first and second electrodes, said resin potting filling a space between said semiconductor chip and said circuit substrate; and

U.S. Patent Application Serial No. 09/768,174

a resin side wall cover covering a side wall of said circuit substrate[;]

said chip having a side wall substantially flush to an outer surface of said resin side wall cover, said side wall of said chip being substantially perpendicular to a principal surface of said chip.